Automatic under Voltage Load Shedding and Automatic Switching of Bus Reactors for Mitigating Fault Induced Delayed Voltage Recovery

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ABSTRACT
This paper presents the application of automatic under voltage load tripping and switching of shunt reactors as counter measures for fault induced delayed voltage recovery (FIDVR). As dynamic behavior of loads has significant impact on simulating FIDVR, proper load modeling is also discussed in this paper. Simulations conducted on actual network show that the proposed load model is effectively able to simulate FIDVR. It also shown that automatic under voltage load shedding and switching of shunt reactors can be used as counter measures for reducing risk of voltage collapse or over voltage conditions that may take place following load tripping caused by FIDVR.

KEYWORDS: Fault Induced Delayed Voltage Recovery, Air Conditioner, Induction Motor, Bus Reactor, Under Voltage Load Shedding

1. INTRODUCTION

Fault induced delayed voltage recovery (FIDVR) is an event in which voltage depression will last for about 5 to 30 seconds following a fault [1]. This slow voltage recovery can cause voltage collapse, massive motor load tripping, temporary over voltage, and subsequently loss of generation due to operation of generator over voltage protection. FIDVR is initiated by a fault on transmission, sub-transmission or distribution system whereby the fault is cleared normally within 3 to 5 cycles; however, voltages remain significantly low for several seconds. It is believed that FIDVR is initiated by stall of constant torque, low inertia induction motors during the fault. These kinds of motors are widely used in single phase air conditioners (A/C) [2]. Therefore, probability of FIDVR in a system and its associated risk is directly related to amount of A/C loads in the system.

The stalled motor draws heavy current from the system which results in low voltage for a period of time and thereby leading to voltage collapse [2]. Low voltage condition for long period may cause generator tripping, or limiting the MVAR output of generators by over excitation limiter and thereby further voltage reduction and finally wide voltage collapse.

Induction motor penetration is one of the most critical parameters that determine a transmission system's susceptibility to FIDVR events. Highly concentrated induction motor loads with constant torque could stall in response to low voltages associated with system faults. FIDVR is worst when there is a concentration of "stall-prone" motors in a region. Not all motors are prone or vulnerable to stalling. For example, large industrial motors often have contactors that will drop the motor out during voltage dips, therefore limiting the negative impact of these motors. Large HVAC units may also have motor protection that will trip the unit offline before stalling occurs. Smaller HVAC units, however, may not have protection that will trip the unit off before stalling occurs. The mechanical torque of the compressor for these units tends to remain relatively constant for the first few seconds which makes the motors more prone to stalling [3]. Susceptibility to FIDVR is also very sensitive to location. A fault at a higher voltage level can depress the voltage over a wider area. Therefore, the potential for voltage to be reduced by a fault over a wide area, coupled with a large concentration of motor load in that area are important factors that indicate the likelihood of a FIDVR occurring. Stalled motors may go out of service due to thermal protection devices. This can result in massive load loss and over voltage condition [4].

Planning studies have not been able to replicate FIDVR events very accurately due to an inaccurate modeling of loads. Uncorrected, this modeling deficiency has a two-fold detrimental effect. First, it can result in studies that do not adequately identify potential FIDVR events. Second, it can give false confidence in mitigation plans designed to prevent FIDVR events [5].

Fig. 1 shows a typical FIDVR event and some of

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its consequences [5]. From this figure, it is observed that following fault clearing, thermal protection may disconnect stalled A/C due to delayed in voltage recovery. Sometimes delay in voltage recovery may even cause local or wide voltage collapse. Subsequent to A/C disconnection, over voltage condition may take place because still capacitors are in service but massive load loss has taken place. This over voltage condition can itself result in generator tripping due to over voltage protection. Sometimes the over voltage condition can be controlled by capacitor tripping or operation of on-load tap changer (OLTC). After this period, the A/C will restart and system will experience under voltage condition because capacitors are out of service and OLTC has operated to control over voltage condition [5]. This under voltage condition may result in another event. Automatic under voltage load shedding and switching of bus reactors can mitigate these conditions and accordingly, improve system stability.

The demand side solutions are effective and economic to undertake FIDVR. Ref. [6] proposes a method for under voltage load shedding based on voltage recovery rate. A MVA-Volt index was proposed for steady-state screening of buses to identify FIDVR in [7]. Ref. [8] Presents an under voltage protection method using 78% of the motor rated voltage as the threshold for stalling protection. Ref. [9] develops a novel online fast load shedding strategy aimed at shedding the most effective load to mitigate FIDVR using the induction motor kinetic energy deviation. In [10] Support Vector Machine (SVM) classifier was used to develop a technique that can predict the transient stability status after a fault.

This paper presents the application of automatic under voltage load tripping and switching of shunt reactors as counter measures for FIDVR. As dynamic behavior of loads has significant impact on simulating FIDVR, proper load modeling is also discussed in this paper. The rest of the paper is as follows:

In section 2, proper load modeling for simulating FIDVR is discussed. In section 3 application of automatic under voltage load shedding and switching of bus reactors is discussed, and in section 4, study methodology is addressed. In section 5 a real system which is prone to FIDVR is simulated and effect of automatic under voltage load shedding and switching of bus reactors for mitigating FIDVR and its consequences is shown.

2. LOAD MODEL

To anticipate the possibility of FIDVR and assess its potential impact on the system, proper load modeling is required [11]. Fig. 2 shows the recorded voltage following a fault on one of substations in Iran south east power network. From this figure it can be observed that the voltage recovery took long time (about 10 seconds) and therefore, the network is prone to FIDVR especially during summer peak due to running huge number of single phase A/C. Studies conducted before, indicated that 60% of the system load during summer peak in the said network is voltage and frequency dependent load and the remaining 40% is prone to stall single phase A/Cs [12].

There are different types of load model. However, for specific type of studies, one type of model may be better than other types. It is also possible that one model which gives good results for a particular type of study may not be suitable for other type of studies.

Fig. 3 shows the schematic diagram of a single phase constant torque low inertia A/C. Different models have been proposes for this type of induction motors [12]. However, for studying effects of A/C on FIDVR, the suitable motor model which can simulate below characteristic should be used:

A) Auto tripping due to under voltage.
B) Motor stalling.
C) Over load thermal tripping.
D) Auto restarting after voltage recovery.

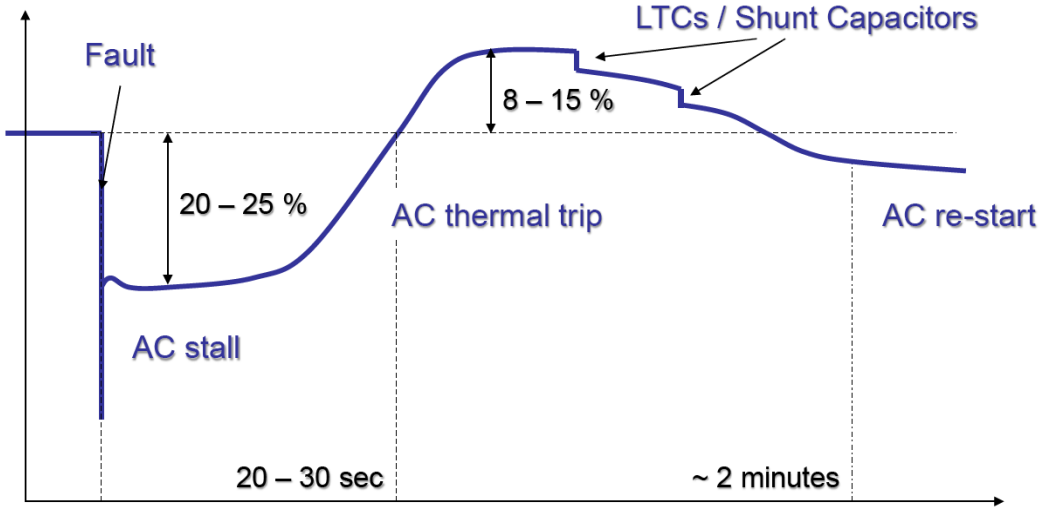

Fig. 1. Typical FIDVR and its associated consequences

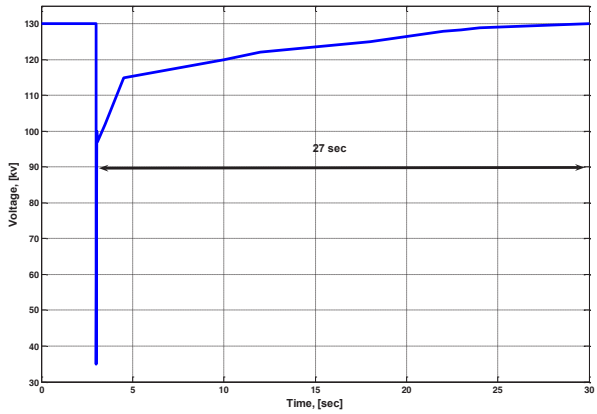

Fig. 2. Recorded FIDVR following a fault on transmission network

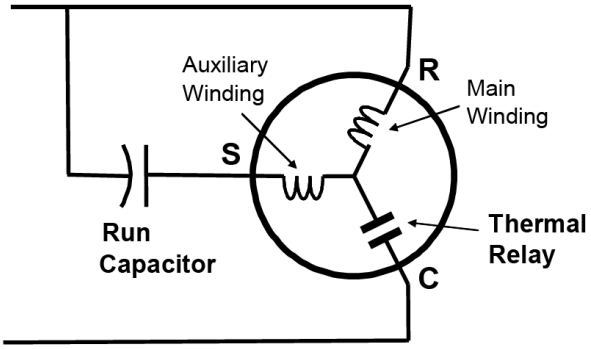

Fig. 3. Single phase, two windings, and capacitor run motor

In this paper, PSS/E software has been used for performing simulations. As standard motor load (CIM) in PSS/E does not consider above mentioned characteristics, therefore, the proposed A/C motor model (ACMTBL) which includes compressors, contactor controls and thermal protection has been used for modeling motor loads. Parameter tunings for this model was done to recapture the incident of Fig. 2 and the final model with tuned parameters was used for simulating FIDVR in Iran south east power network.

3. AUTOMATIC UNDER VOLTAGE LOAD SHEDDING AND SWITCHING OF BUS REACTORS

Besides faster clearing fault and using FACTS devices [8], proper under voltage load shedding and switching of bus reactors can mitigate FIDVR and its associated consequences in three ways which can be best understood by referring to Fig. 1.

1- Under Voltage: following fault clearance, reactors can automatically be switched off (if it is already in service) and load can be shed (if voltage collapse is anticipated) to boost voltage and make voltage recovery faster, and finally reduce risk of voltage collapse or A/C stall.

2- Over Voltage: automatic insertion of bus reactors can limit voltage overshoot resulted from load tripping. Limiting voltage overshoot can prevent damage to equipment and avoid generator tripping due to over voltage condition.

3- Under Voltage: after tripped A/Cs are reconnected to the system gradually, automatic tripping of bus reactors can control voltage drop and minimize risk of cascading events [12]. The relay which is suitable for automatic switching of bus reactors should normally have more than one stage and must operate only when all three voltages are above or below the threshold level or the relay should operate based on positive sequence voltage [13]. Under voltage/ over voltage settings and related time delays should be selected after simulating different scenarios and disturbances. However, as a guideline, under voltage settings for tripping of bus reactors should be in the range of 0.9 p.u to 0.95 p.u and its related time delay should be in the range of 1 to 5 seconds. The settings for over voltage insertion of bus reactors should be in the range of 1.1 p.u to1.15 p.u with time delays in the range of 5 to 10 seconds. Also, to avoid unnecessary load disconnection, priority should be first given to automatic switching of bus reactors before starting under voltage load shedding.

4. STUDY METHODOLOGY

For studying FIDVR and its consequences, dynamic simulation is required. As load model especially model of motor loads which are prone to stall plays a significant role in FIDVR simulation, motor loads should be modeled carefully. For other loads, voltage and frequency dependent load model may be used. Generators and their controllers such as exciter, governor and PSS should also be properly modeled. Moreover, especial attention should be paid to modeling of under excitation and over excitation limiters along with generator over voltage protection while studying FIDVR [14]. As the percentage of motor load during peak period is more than the percentage of motor load during off peak period, peak load condition is worse than off peak load condition for FIDVR event, therefore, peak load condition should be used for FIDVR simulations.

After preparing suitable model, potential FIDVR locations should be identified. This can be done using time domain simulation by applying fault with normal clearing time at various locations and then monitoring system voltage [15]. If undesirable voltage profile or delay in voltage recovery is observed, proper counter measures (such as automatic under voltage load shedding and switching of bus reactors) should be provided. To find proper voltage and time settings for above counter measures, voltage stability limits (both over voltage and under voltage) for the network should be first specified [16]. Stability limits should be such that:

A) Voltage collapse is avoided.
B) As far as possible, motor stall is avoided.
C) Generator tripping due to over voltage condition is avoided.
D) Transformer over excitation or equipment damage due to over voltage condition is avoided (over voltage condition may happen in case of

motor load tripping).

It should be noted that above voltage stability limit depends on over voltage/ under voltage protection settings for generators, capacitors, transformers, etc., and is varying from one utility to another utility [17]. For example, for the network under study in this paper, voltage stability limits are as below:

A) Voltage should not remain below 0.80 p.u for more than 0.4 seconds
B) Voltage should not remain below 0.9 p.u for more than 2 seconds.
C) Voltage should not remain above 1.15 p.u for more than 5 seconds.
D) Voltage should not remain above 1.2 p.u for more than 1 second.

In view of above, automatic under voltage load shedding and switching of bus reactors should be designed to fulfill desired voltage stability limits.

5. SIMULATION RESULTS

Iran south east power network has been selected for simulation. The single line diagram of the network is shown in Appendix and the complete system data not shown here can be obtained in [18]. The voltage and frequency dependency coefficients of the loads for the network under study are as follows [18].

$$\begin{aligned} P &= P_{load}(a_1 V^{n_1} + a_2 V^{n_2} + a_3 V^{n_3}) \\ &\quad \times (1 + a_7 \Delta f) \\ Q &= Q_{load}(a_4 V^{n_4} + a_5 V^{n_5} + a_6 V^{n_6}) \\ &\quad \times (1 + a_8 \Delta f) \end{aligned} \quad (1)$$

where, P_{load} and Q_{load} are the real and reactive power loads that would be drawn at nominal frequency and one per unit voltage. The corresponding values of the parameters a_i and n_i are as follows [18]:

$$\begin{aligned} &a_1 = a_2 = a_3 = a_4 = a_5 = a_6 = 0.33\text{p.u.} \\ &a_7 = a_8 = 0.1\text{p.u.} \\ &n_1 = n_4 = 0, n_2 = n_4 = 1\text{p.u.} \\ &n_3 = n_6 = 2\text{p.u.} \end{aligned} \quad (2)$$

The aim is to use under voltage load shedding along with automatic switching of capacitors and bus reactors as counter measures for FIDVR. Detailed models for generators, governors, exciters, PSS, over voltage protection of generators, over excitation limiter (OEL) and under excitation limiter (UEL), shunt reactors and capacitors have been considered. System load is divided into two parts: 40 percent induction motor (due to air conditioners and district cooling systems) and 60 percent static load with frequency and voltage dependency characteristic. ACMTBL model in PSS/E was used for modeling A/C loads and actual incident shown in Fig.2 has been used for fine tuning of A/C model.

Initially, three phase faults with the duration of 100ms have been applied at various locations and potential FIDVR locations have been identified. As an example, Fig.4 shows a sample of voltage profile for some buses in the network for a three phase fault on bus 4. From this figure it is observed that depends on the distance to the fault location, voltage is remaining substantially low at some buses while it is recovering very fast at some others. So, local voltage collapse is expected because stalled motors remained connected to the network.

Voltage profiles similar to those shown in Fig. 4, were obtained for different buses for faults on various locations, and potential FIDVR locations were identified. In the next step, automatic switching of bus reactors was designed as per Table 1 to meet voltage stability limit.

	Voltage (p.u)	Time Delay (s)	Voltage (p.u)	Time Delay (s)
Under Voltage	0.9	1	0.95	5
Over Voltage	1.15	5	1.1	10

Table 1. Settings for automatic switching of bus reactors

For designing under voltage load shedding, following steps are required:

A) Determination of the amount of load to be tripped
B) Selection of loads to be dropped
C) Determination of time steps of load tripping
D) Determination of voltage level at which shedding begins.

Guidelines mentioned in [19] were used for designing under voltage load shedding in Iran south east network. Table 2 summarizes the proposed under voltage load shedding scheme.

	Voltage (p.u)	Time Delay (s)	Load Shedding (%)
Stage 1	0.80	0.4	2.5
Stage 2	0.90	2.0	5.0
Stage 3	0.92	5.0	5.0
Stage 4	0.92	8.0	5.0

Table 2. Settings for under voltage load shedding

Fig. 5 shows a sample of voltage profile for some buses in the network for a three phase fault at one location after implementing both automatic under voltage load shedding and switching of bus reactors and capacitors. It was assumed that 3 numbers of bus reactors, each one rated as 40MVAR and 2 numbers of shunt capacitors, each one rated as 10MVAR are available for switching operations. From Fig.5 it is observed that automatic under voltage load shedding and switching of bus reactors and capacitors effectively mitigated FIDVR and prevented risk of voltage collapse.

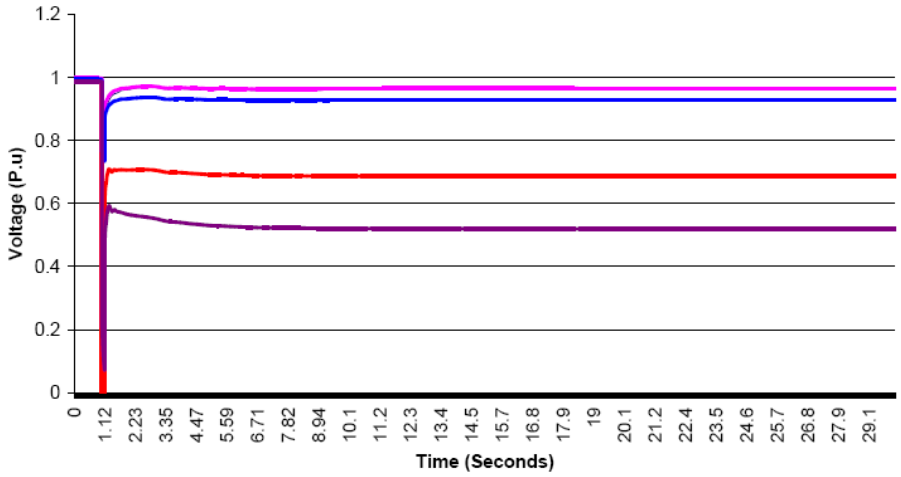

Fig. 4. Voltage of some buses for a three phase fault

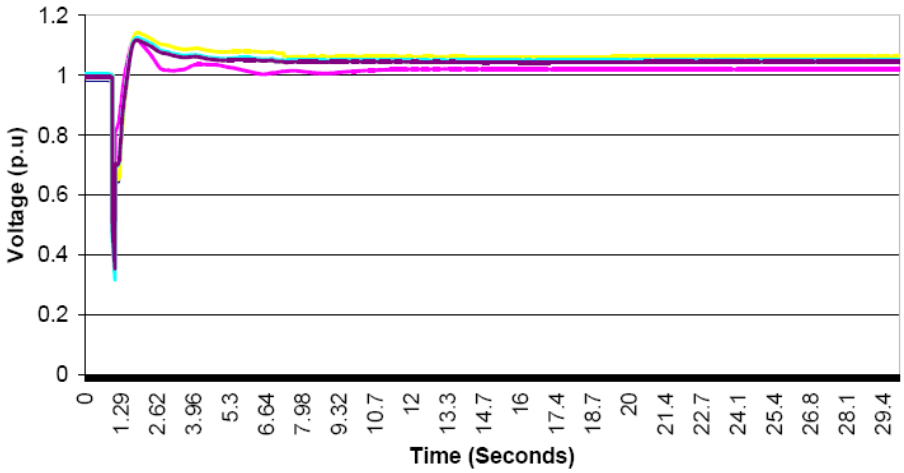

Fig. 5. Voltage of some buses for a three phase fault

6. CONCLUSION

Dropping voltage to below voltage stability limits during large disturbances can result in induction motor stalling. If stalled motors remain connected to system, they absorb high reactive power which can cause voltage collapse. Moreover, air conditioners previously disconnected due to over load thermal protection are automatically restarted gradually and draw a large starting reactive current from the network. Air conditioners are single phase, constant torque low inertia induction motors which in case of voltage drop, their electrical torque will reduce to below the mechanical load torque and motor will stall. In this paper, it was shown that Iran south east network is prone to voltage collapse due to utilizing huge number of air conditioners during summer period. To reduce risk of FIDVR and its consequences, automatic under voltage load shedding and switching of bus reactors were proposed. Simulation results showed that the proposed scheme can effectively mitigate FIDVR and subsequent voltage collapse.

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APPENDIX:

The single line diagram of the network under study is shown in Fig. A1 [18].

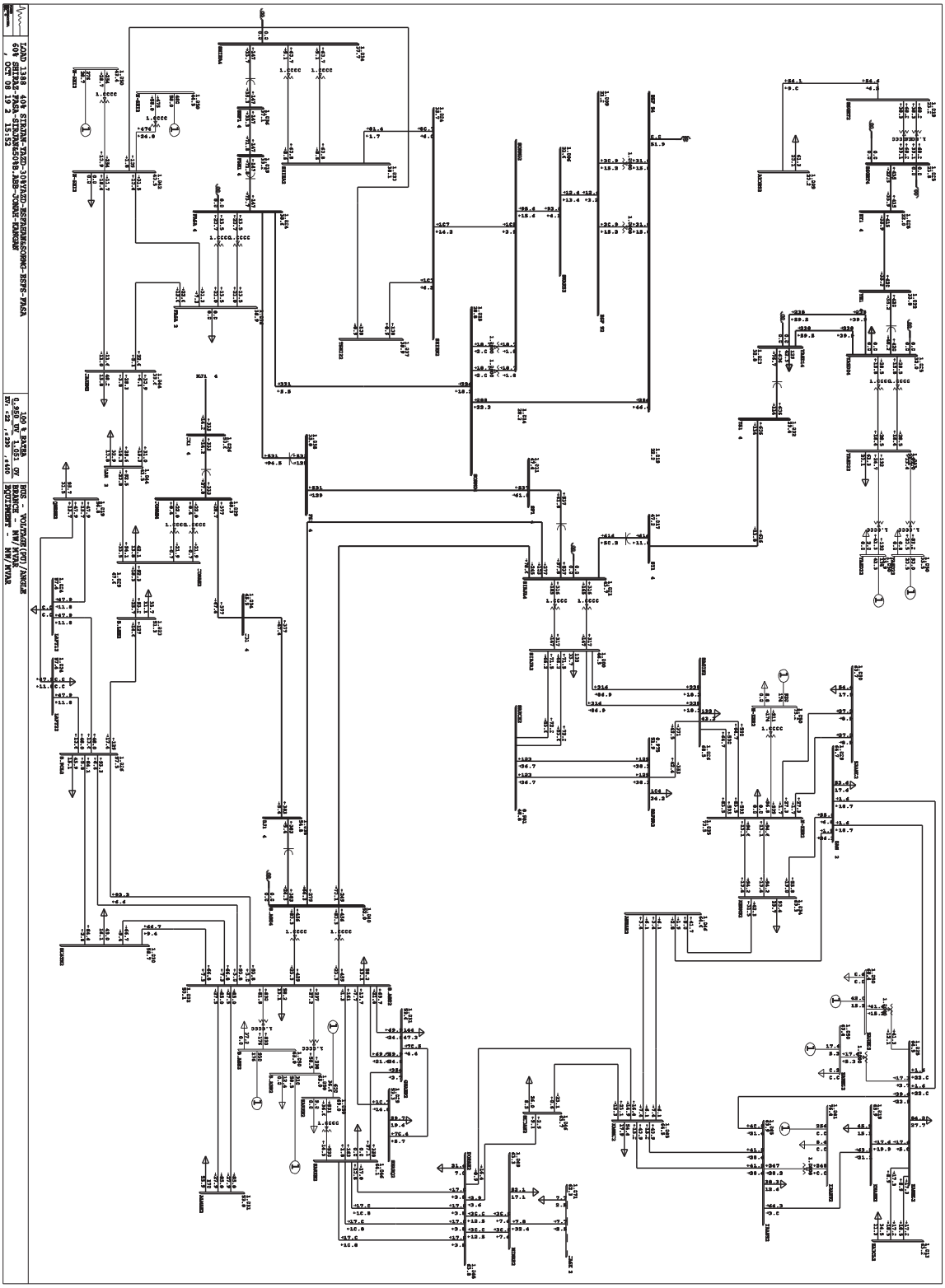

Fig. A1: Single-line diagram of the network under study.